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CHANNEL SELECT MEMORY. (U)

JUL 76 W PECK F33615-75-C-1108

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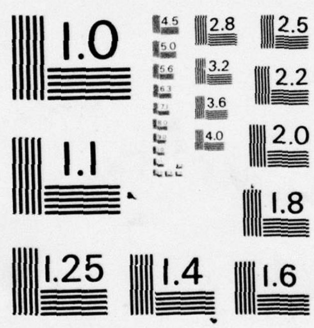

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AFAL-TR-75-213

(12)

CHANNEL SELECT MEMORY MODULE

ELECTRICALLY PROGRAMMABLE, NON-VOLATILE, SEMICONDUCTOR MEMORY ORGANIZED SIXTEEN-BIT PARALLEL X32 WORDS

ELECTRONIC COMMUNICATIONS, INC.
1501 - 72ND ST., N.
ST. PETERSBURG, FLORIDA 33710

AIR FORCE AVIONICS LABORATORY

JULY 1976

TECHNICAL REPORT AFAL-TR-75-213

FINAL REPORT FOR PERIOD NOVEMBER 1974 – JULY 1975

AIR FORCE AVIONICS LABORATORY
AIR FORCE WRIGHT AERONAUTICAL LABORATORIES
Air Force Systems Command
Wright-Patterson Air Force Base, Ohio 45433

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19 REPORT DOCUMENTATION PAGE

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18. SUPPLEMENTARY NOTES

19. KEY WORDS (Continue on reverse side if necessary and identify by block number)

Electronic equipment memory device, metal-nitride-oxide-silicon, preset memory, nonvolatile, electrically alterable, fully decoded, 16 bit-32 words, parallel inputs/outputs, TTL, and CMOS compatible

20. ABSTRACT (Continue on reverse side if necessary and identify by block number)

A fully decoded 512-bit (32 x 16) MNOS electrically word alterable, semiconductor memory was developed for use in channel preselect applications to control the frequency in UHF communication systems. It includes address and timing buffers, row decoders, column detectors, and input/output circuitry. Packaged in a standard 28-pin dual inline ceramic package, the memory characteristics are: (1) electrically erasable by word, (2) 100 milliseconds erase and write time, (3) 8 microseconds read time, (4) 2×10^{11} read (CONT'D)

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20. accesses/word between refreshes, (5) unpowered nonvolatile data storage one-year minimum, (6) common data inputs/outputs compatible with 400 series CMOS and 5400 TTL, (7) data outputs high impedance when memory deselected, (8) operating temperature -55°C to +125°C, (9) power supply requirements of 5 volts ±.5 volt DC and 28 volts ±1.5 volts DC at 10 milliamps maximum current.

A small quantity of memories selected from three production lots to demonstrate reproducibility were delivered to AFAL. Prior to shipment, a design and device parameter test program was conducted to verify conformance to the above parameters.

PREFACE

This report was prepared by Wayne P. Peck, Electronic Communications, Inc., St. Petersburg, Florida. The memory was designed and fabricated at NCR's Microelectronics Division located in Miamisburg (Dayton), Ohio. Dr. Wendel Spence was the Project Coordinator at NCR and George C. Lockwood was the Project Engineer responsible for the design and development of the memory at NCR . The developed memory, NCR 2050, was accomplished under Contract Number F33615-75-C-1108, during the period November 1974 through July 1975. The AFAL/TEA Project Engineer was Dr. F. L. Schuermeyer, and the AFAL/TEA Memory Technology Group Manager responsible for the project was John M. Blassingame.

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Introduction

An electrically programmable, non-volatile semiconductor memory organized 16-bit parallel x 32 words was developed by this program. The main objective of this program was to develop a memory for use in channel preselect applications to control the frequency in UHF communication systems. Core memories are presently being used in channel preselect applications; a semiconductor memory would permit cost and power reduction and would increase reliability. This development program resulted in the design, fabrication, and characterization of fifty 28-pin dual in-line integrated circuit memories. Producibility of these circuits was demonstrated by fabricating these parts from three separate production lots, thus, insuring that parts from future lots will have similar and predictable characteristics.

Task

A fully decoded, 512-bit (32x16) MNOS electrically alterable read only memory was developed. The memory includes address buffers, timing buffers, row decoders, column detectors, and input/output circuitry. The features of this integrated circuit memory are:

a. Electrically Programmable
b. Electrically Erasable by Word
c. Sixteen-bit Parallel x 32 Word Organization
d. 100MS Erase Time
e. 100MS Write Time
f. Eight Microsecond Read Time
g. Words are capable of 2×10^{11} Read Access/Word Between Refreshes
h. Unpowered Non-volatile Data Storage One Year Minimum
i. All Inputs and Outputs Compatible with 4000 Series CMOS
j. Common Data Input/Output
k. Data Outputs are High Impedance when Memory Deselected
l. Power Supply +5 Volts ±.5 Volts DC and 28 Volts ±1.5 Volts DC at 10 MA Maximum
m. Operating Temperature -55°C to +125°C

The memory is mounted in a 28-pin DIP ceramic package. Pin count and functions are:

a. Common Data Input/Output--16 pins CMOS Compatible 5 Volt Supply
b. Address------------------ 5 pins CMOS Compatible 5 Volt Supply
c. Mode Control (read/write/erase, chip select)--------- 3 pins CMOS Compatible 5 Volt Supply
d. Clock -------------------- 1 Pin CMOS Compatible 5 Volt Supply
e. Substrate ---------------- 1 Pin +5 Volts ±.5 Volts @ 10 MA Max
f. Power Supply------------- 1 Pin -28 Volt ±1.5 Volts @ 10 MA Max
g. Ground------------------- 1 Pin

Fifty fully operational memories were delivered to AFAL/TEA-3. These memories were selected from three different fabrication lots with at least ten memories selected from each of the three fabri-

cation lots. Each of the fifty memories delivered to AFAL were functionally tested over the full military temperature range, -55°C to +125°C, at minimum, nominal, and maximum power supply voltages.

Design Verification

The memories were electrically evaluated to obtain the read time, write time, erase time, retention and endurance. (See Tables 1 through 5 for these electrical characteristics.) The operating limits over the temperature range from -55°C to +125°C are given in Table 1. Power supply current is plotted versus temperature and voltage for reading and writing in Table 2, Figures 1 and 2. Data output current capability for a fixed output level of 0.8 Volts is plotted versus temperature and power supply voltage in Table 2, Figure 3. Peak power dissipation during writing is plotted versus temperature and power supply voltage in Table 2, Figure 4. Volatility measurements are plotted in Tables 3, 4, and 5. The volatility measurements indicate that retention is greater than one year in a 125°C ambient. A memory word was subjected to 1.1×10^6 write-erase cycles at 125°C to confirm the 10^6 write-erase endurance requirement. The written word was still alterable and the remainder of the memory still contained the initial data. To confirm the 2×10^{11} read accesses/word between refresh requirement, a memory word was read in excess of 2×10^{11} times. The read word was unaltered and the remainder of the memory still contained the initial data.

Device Verification

The fifty devices shipped were functionally verified by test. A memory exerciser was specially designed and constructed for this purpose.[1] The exerciser is constructed to test ten memory devices at a time. The ten memories are inserted into a test board, which is pluggable through a patch cable into the memory exerciser. Three test boards and patch cables were constructed to permit testing of thirty memory devices in a batch. Thus, the three test boards can be placed into an environmental chamber to permit thirty devices to be temperature tested, at one time. The test boards are plugged one at a time into the exerciser for a sequence of tests. Normally, the exerciser is operated in the automatic mode in which the operator initiates an automatic sequence of tests by depressing the "write" push button. The exerciser will also manually write or read a single word selected by the operator. When in manual mode, the operator can write any desired bit pattern into any word in a selected memory, just as an operator would if the memory were actually in a control box application. Automatic exerciser operation is as follows:

1. A pattern is written into the memories one word at a time, sequencing through the 32 words. Thus, the pattern is written into 32 words of the memory and all 16 bits of each word. This writing sequence occurs simultaneously for all ten devices on the test card.

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1. The memory exerciser was designed and constructed on an ECI IR&D Program for purposes of expediting the device testing on the AFAL Program.

Device Verification (Continued)

2. The test pattern is then read, starting with the first memory and the first word, sequencing through the 32 words of the first memory. The exerciser then steps to the next memory and sequences through its 32 words. This process is then repeated until all ten memory devices are read. All 16 bits in each word read are compared against the pattern written into the memory. In the event that a bit is read incorrectly, the exerciser halts the sequence, illuminates an error indicator and displays the device number, word number and bit pattern read. The operator can verify the error and continue the sequence to check for other discrepancies.

3. Steps 1 and 2 are repeated for each of four patterns. The four patterns written into and read from the memories are:

   a. All Zeros
   b. All Ones
   c. Checkerboard (10 even words, 01 odd word)
   d. Inverse Checkerboard (01 even word, 10 odd words)

4. Steps 1, 2 and 3 are repeated for each of three power supply voltages. The three power supply voltages are:

   a. Nominal ----- 28 Volts DC
   b. High -------- 29.5 Volts DC
   c. Low -------- 26.5 Volts DC

5. Steps 1, 2, 3 and 4 are repeated for each of two clock pulse widths. The clock pulse widths are:

   a. 0.5 usec
   b. 1.0 usec

6. Steps 1, 2, 3, 4 and 5 are repeated for each of three ambient temperatures. The ambient temperatures are:

   a. 125°C
   b. 25°C
   c. -55°C

A block diagram of the test sequence is shown in Figure 1 and a block diagram of the memory exerciser is shown in Figure 2. Test results are summarized in Tables 6 through 9. Note: All devices were functionally tested by NCR at room temperatures with a Fairchild Sentry I. C. test station prior to the full temperature range tests.

Functional Information

The memory has four modes of operation ---------read, hold, write, and erase. These modes are selected by applying the logic levels shown in Table 10 to Control 1 and Control 2. The mode of operation affects only the word addressed by a 5-bit binary word, applied to the address inputs.

Data is either available at the 16 data/bi-directional pins in read mode or applied to the 16 bi-directional data pins in write mode. Data outputs go directly to the correct state and are glitch free during multiple reads. Data outputs change within one microsecond of each other.

Figure 3 illustrates the suggested timing relationships between the control logic levels and the data input/output logic levels. Only one clock pulse is required during each read operation; the clock may be present at all times or may be absent during hold, write or erase if the clock is held low (Vcc). The clock pulse should be high (Vss) for a minimum of one microsecond and should have a minimum repetition rate of 10 microseconds between transitions.

Chip select is a control signal which can be used to deactivate the memory to permit multiple memories to be wire OR'd together and selected one at a time, or which can be used to deactivate the memory when control signals are uncertain during power up or power down. When chip select is low (Vcc) the memory cannot be erased or written regardless of the state of Control 1 and Control 2. Figure 4 is a block diagram of the memory circuitry which can be used to interpret the schematic diagram of the memory circuitry shown in Figure 5.

Summary

The objective of this program to design, to develop and to fabricate a fully decoded MNOS electrically alterable read only memory chip for the purpose of demonstrating the technical feasibility of this type of memory in the Air Force Systems was met. The EROM, developed in this program, can be used in channel preselect memory applications to reduce cost, power and size from the presently utilized core memories. The EROM developed is more compatible with T^2L and CMOS logic devices than core memories, permitting simpler external circuits to utilize the memory. The reliability of channel preselect memories using the EROM memory is inherently as reliable as any integrated circuit device and is not subject to the failure mechanisms of magnetic memories such as wire breakage due to mechanical stress induced by vibration, shock and thermal cycling.

TABLE 1. EROM ELECTRICAL CHARACTERISTICS

I. OPERATING LIMITS: -55°C TO +125°C ALL PARAMETERS EXCEPT ONE UNDER TEST ARE AT NOMINAL.

PARAMETER	MAX.	TYP.	MIN
V_{GG} WRITE-ERASE	-26	-28	-30
V_{GG} READ	-26	-28	-30
V_{SS}	+5.5	+5.0	+4.5
V_{CC}		0	
ADDRESS HIGH	+5.3	+5.0	+2.6*
ADDRESS LOW	+0.8	0	-10
CONTROL 1 LOW	+0.8	0	-10
CONTROL 1 HIGH	+5.3	+5.0	+2.7*
CONTROL 2 LOW	+0.8	0	-10
CONTROL 2 HIGH	+5.3	+5	+2.4
CHIP SELECT LOW	+0.8	0	-10
CHIP SELECT HIGH	+5.3	+5.0	+3.0*
DATA INPUT LOW	+0.8	0	-10
DATA INPUT HIGH	+5.3	+5.0	+2.4
CLOCK LOW	+0.8	0	-10
CLOCK HIGH	+5.3	+5.0	+2.5*
CLOCK WIDTH		1 μs	800 ns
ACCESS TIME		6 μs	6 μs
POWER	300 MW	200 MW	

*THESE PARAMETERS DO NOT MEET THE MINIMUM TTL HIGH LEVEL OF +2.4V AT 125°C. AT 25°C ALL PARAMETERS EXCEPT CHIP SELECT HIGH MEET MINIMUM TTL REQUIREMENTS.

TABLE 2. EROM ELECTRICAL CHARACTERISTICS

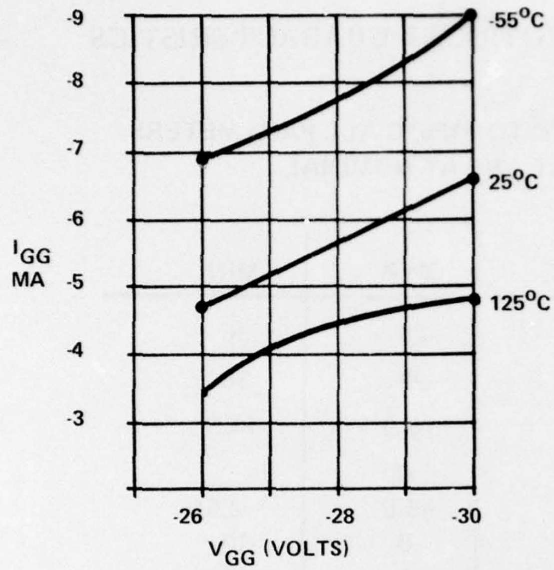


FIGURE 1. I_{GG} WRITE VERSUS V_{GG}
$V_{SS} = +5$

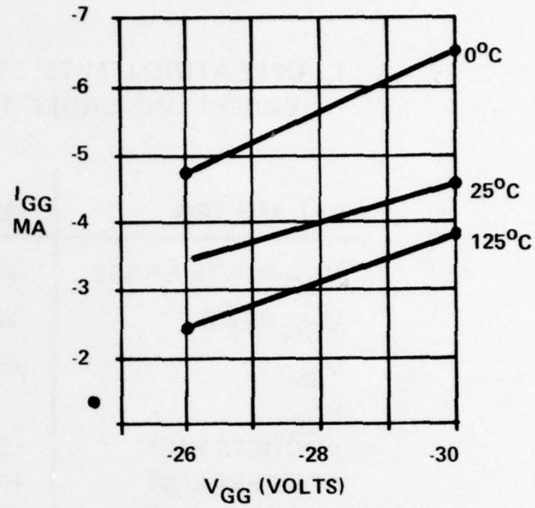


FIGURE 2. I_{GG} READ VERSUS V_{GG}
$V_{SS} = +5$

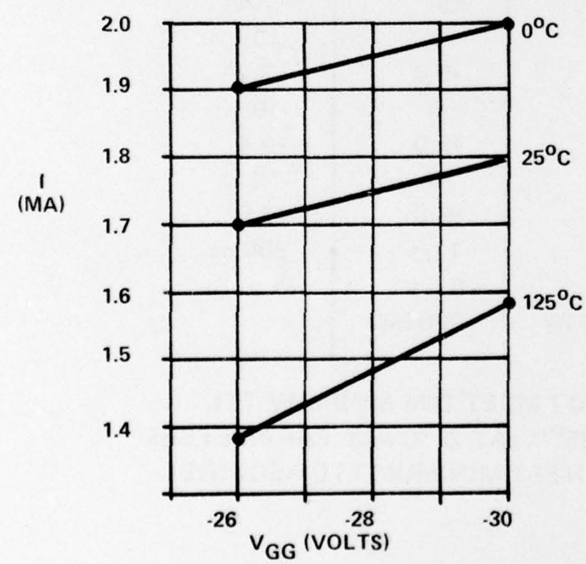


FIGURE 3. OUTPUT TTL 'O' CURRENT
$V_{OUT} = +0.8$ V

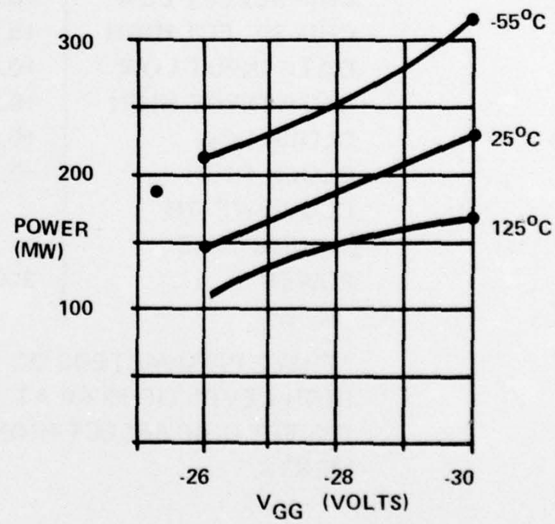


FIGURE 4. MAX POWER DISSIPATION
VERSUS V_{GG} $V_{SS} = +5$

TABLE 3. LIFE VOLATILITY TEST RESULTS

NCR 2050 TEST – VOLATILITY TEST (100 MS, +22V / 100 MS -22V) DATE 24 JUNE 1975

DEVICE 1, 2, 3, 4, 5 TEMP – 125°C

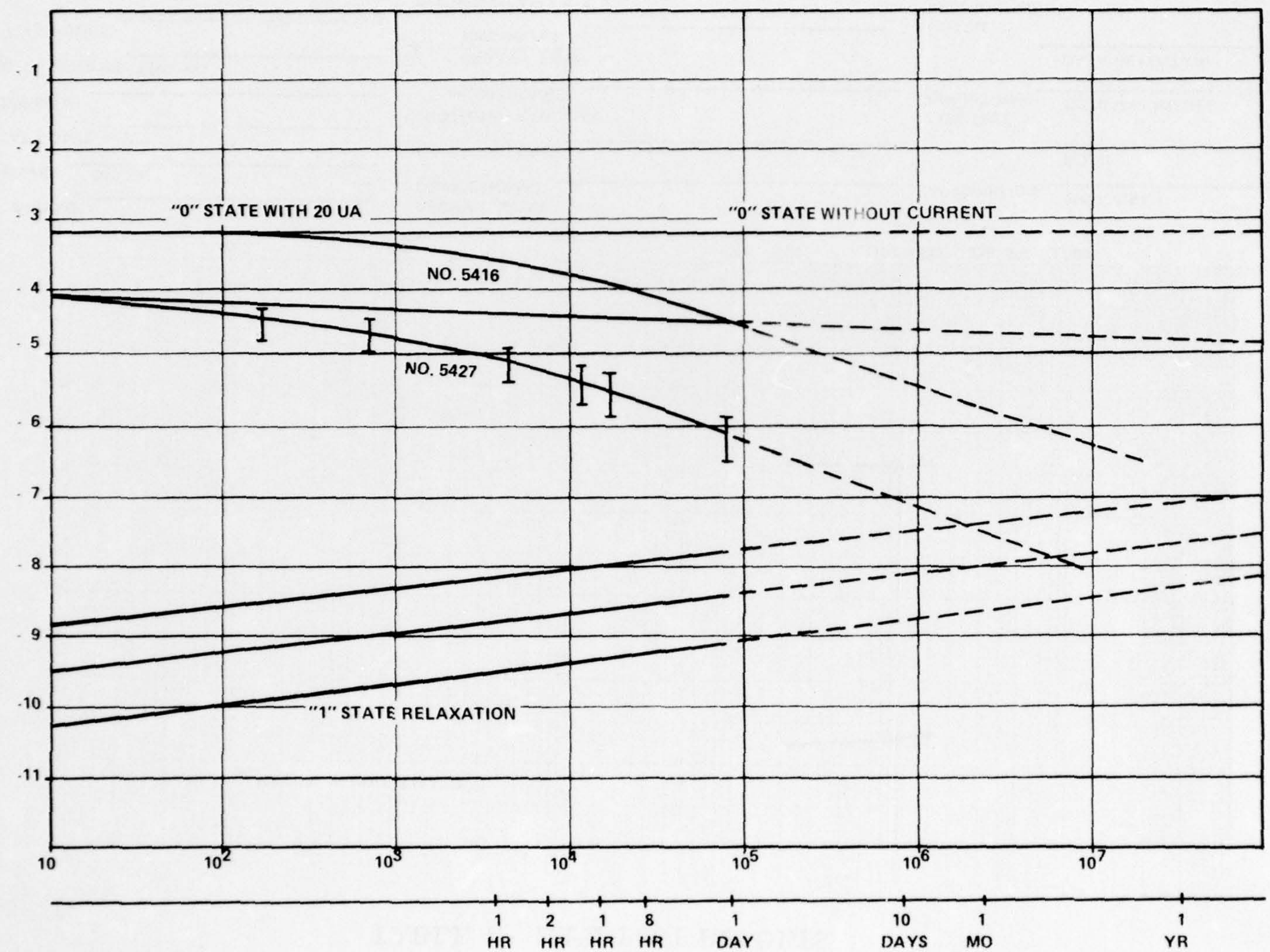
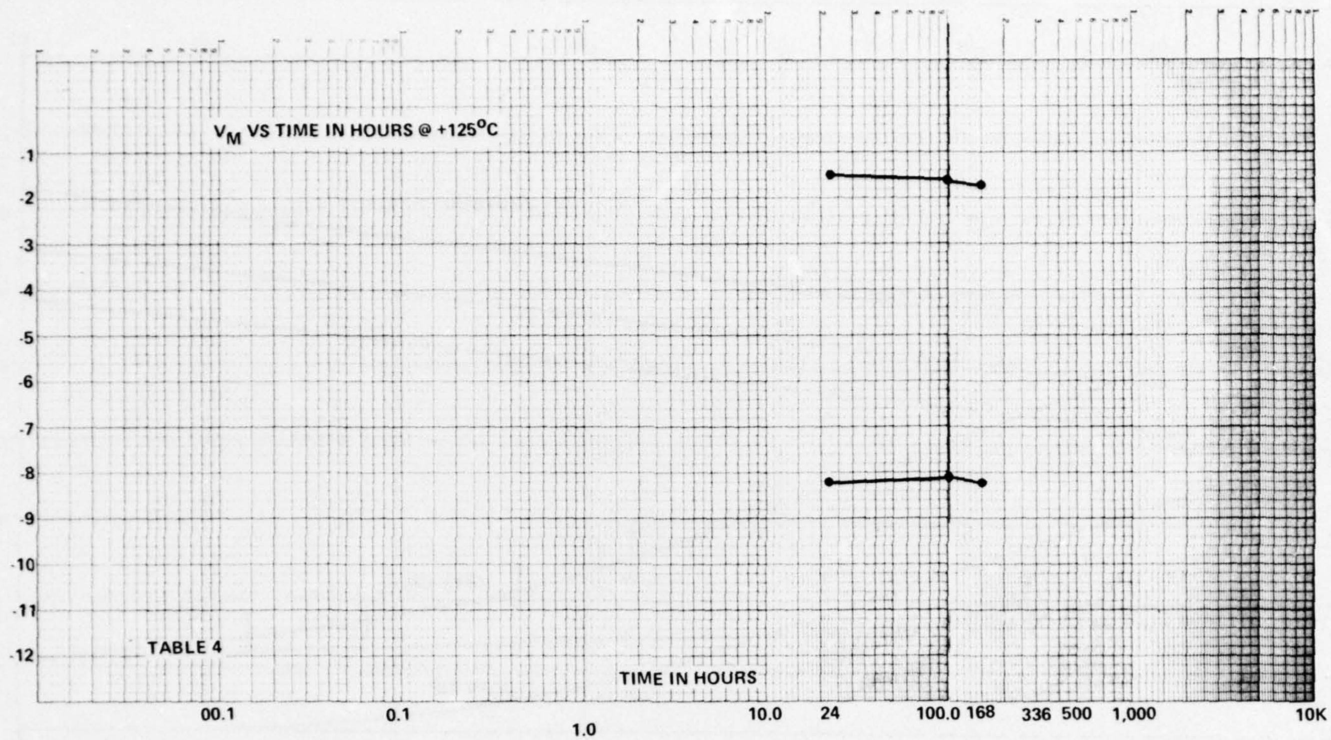


TABLE 4. LIFE TEST RESULTS



BOARD NO. ______

RUN NO. 5413-2

START DATE 6-20-75

STOP DATE ______

NO. OF DEVICES 1 NO. 12

TOTAL HOURS ______

ACCUMULATIVE DEVICE HOURS ______

NO. OF FAILURES ______

PROJECTED FAILURES AT 100,000 HOURS ______

$\lambda = \frac{\text{FAILURE RATE}}{\text{1000 HOURS}}$ ______

PROJECTED FAILURE RATE AT 100,000 HOURS ______

FAILURE ANALYSIS ______

DEVICE DESCRIPTION 2050 TUNER

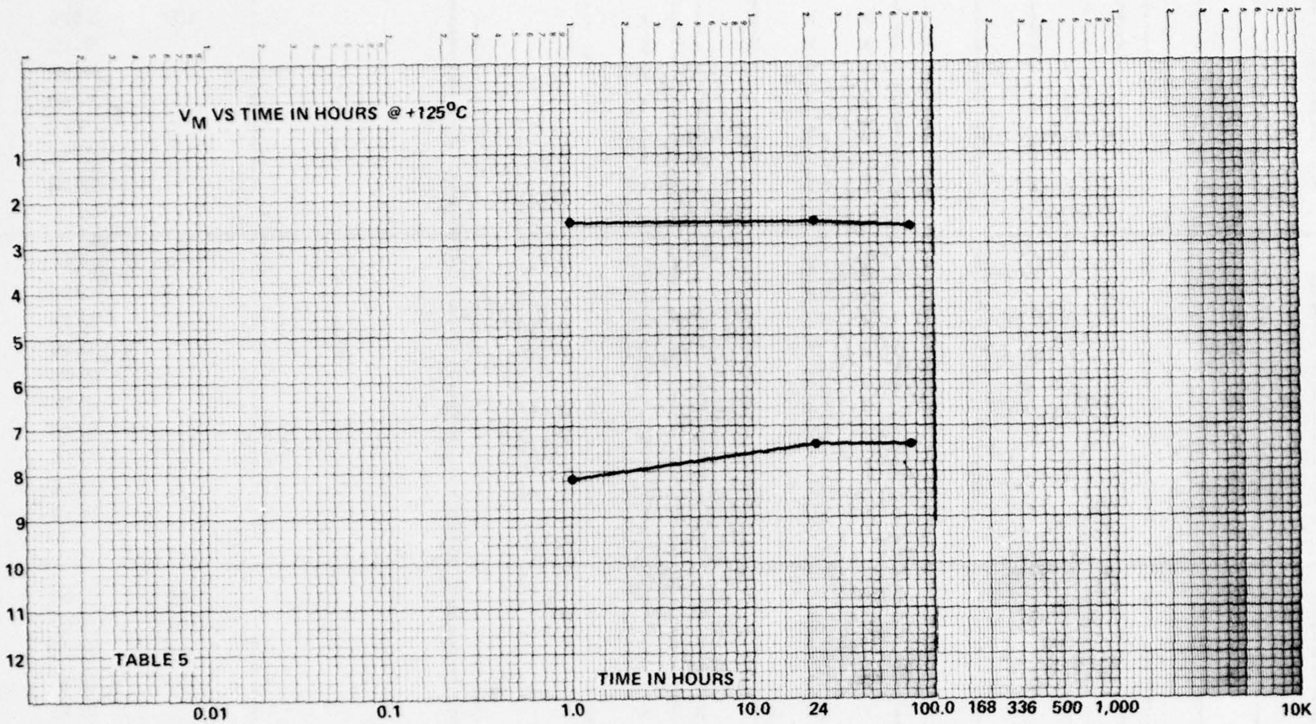
NO. 12

LIFE TEST CONDITIONS 125°C UNPOWERED

DATA RETENTION

INITIAL PROGRAMMING CONDITIONS ______

TABLE 5. LIFE TEST RESULTS



BOARD NO. ________

RUN NO. 5413-2

START DATE 6-24-75

STOP DATE ________

NO. OF DEVICES 1 NO. 0

TOTAL HOURS ________

ACCUMULATIVE DEVICE HOURS ________

NO. OF FAILURES ________

PROJECTED FAILURES AT 100,000 HOURS ________

$\lambda = \frac{\text{FAILURE RATE}}{\text{1000 HOURS}}$ ________

PROJECTED FAILURE RATE AT 100,000 HOURS ________

FAILURE ANALYSIS ________

DEVICE DESCRIPTION 2050 TUNER

NO. 0

LIFE TEST CONDITIONS 125°C UNPOWERED

DATA RETENTION

INITIAL PROGRAMMING CONDITIONS ________

TABLE 6. TEST RESULTS BATCH NO. 1

				25°C				70°C				125°C				0°C				-55°C			
3				28	29.5	26.5	25	28	29.5	26.5	25	28	29.5	26.5	25	28	29.5	26.5	25	28	29.5	26.5	25
				A	B	C	D	A	B	C	D	A	B	C	D	A	B	C	D	A	B	C	D
0	8	5428												X	X								X
1	9	5428													X								
2	10	5428													X								
3	29	5416									X			X	X								
4	30	5416									X			X	X								
5	31	5416									X	X		X	X								
6	37	5427	ECI												X								
7	38	5427	ECI											X	X								
8	39	5427	ECI												X								
9	C	5413	ECI												X								
2																							
0	5	5428												X	X								
X1	6	5428												X	X								
2	7	5428													X								
X3	24	5416									X			X	X								
4	25	5416													X								
5	26	5416									X			X	X								
6	28	5416									X	X		X	X								
7	35	5427	ECI											X	X								
8	36	5427	ECI											X	X								
9	B	5413	ECI											X	X								
1																							
0	1	5428													X								
1	3	5428													X								
2	4	5428													X								
3	21	5416									X			X	X								
4	22	5416									X			X	X								
5	23	5416									X	X	X	X	X								
6	32	5427	ECI								X			X	X								
7	33	5427	ECI											X	X								
8	34	5427	ECI												X								
9	A	5413	ECI											X	X								

NOTE: DEVICES DELIVERED TO AFAL ARE DESIGNATED BY AF AFTER LOT NO.

TABLE 7. TEST RESULT BATCH NO. 2

				25°C				70°C				125°C				0°C				-55°C			
3				28	29.5	26.5	25	28	29.5	26.5	25	28	29.5	26.5	25	28	29.5	26.5	25	28	29.5	26.5	25
0	15	5428-2																					
1	16	5428													X								
2		5428																					
3	18	5428													X								
4	19	5428-2																					
5	41	5427-4													X								
6	42	5427																					
7	43	5427																					
8		5427													X								
9	45	5427-4													X								
2																							
0	2	5428-2													X								
1	69	5428													X								
2	12	5428													X								
3	13	5428-2													X								
4	70	5427-4													X								
5	46	5427-4	AF												X								
6	47	5427	AF												X								
7	48	5427	AF												X								
8	78	5427	AF												X								
9	50	5427-4	AF												X								
1																							
0	51	5427-4	AF												X								
1	60	5427	AF												X								
2	61	5427	AF												X								
3	62	5427	AF												X								
4	63	5427-4	AF												X								
5	64	5428-2													X								
6	65	5428													X								
7	66	5428													X								
X8	67	5428													X								
9	68	5428-2													X								

NOTE: DEVICES DELIVERED TO AFAL ARE DESIGNATED BY AF AFTER LOT NO.

TABLE 8. TEST RESULT BATCH NO. 3

				25°C				70°C				125°C				0°C				-55°C			
3				28	29.5	26.5	25	28	29.5	26.5	25	28	29.5	26.5	25	28	29.5	26.5	25	28	29.5	26.5	25
0	80	5413-5	AF												X								
1	110	5413-5	AF												X								
2	82	5413-5	AF											X	X								
3	83	5413-5	AF											X	X								
4	84	5413-5	AF												X								
5	85	5416-2	ECI												X								
6	86	5416-2	ECI												X								
7	87	5416-2	ECI												X								
8	88	5416-2	ECI											X	X								
9	89	5416-2	ECI											X	X								
2																							
0	90	5413-5	AF											X	X								
1	111	5413-5	AF												X								
2	92	5413-5	AF												X								
3	93	5413-5	AF												X								
4	94	5413-5	AF											X	X								
5	95	5416-2	ECI											X	X								
6	96	5416-2	ECI												X								
7	97	5416-2	ECI											X	X								
8	98	5416-2	ECI											X	X								
9	99	5416-2	ECI												X								
1																							
0	100	5413-5	ECI												X								
1	112	5413-5	ECI												X								
2	102	5413-5	ECI											X	X								
3	103	5413-5	X												X		X	X	X	X	X		X
4	104	5413-5	ECI											X	X								
X5	105	5416-2	X											X	X			X	X	X	X		X
6	106	5416-2	ECI											X	X								
7	107	5416-2	ECI												X								
8	108	5416-2	ECI											X	X								
9	109	5416-2	ECI											X	X								

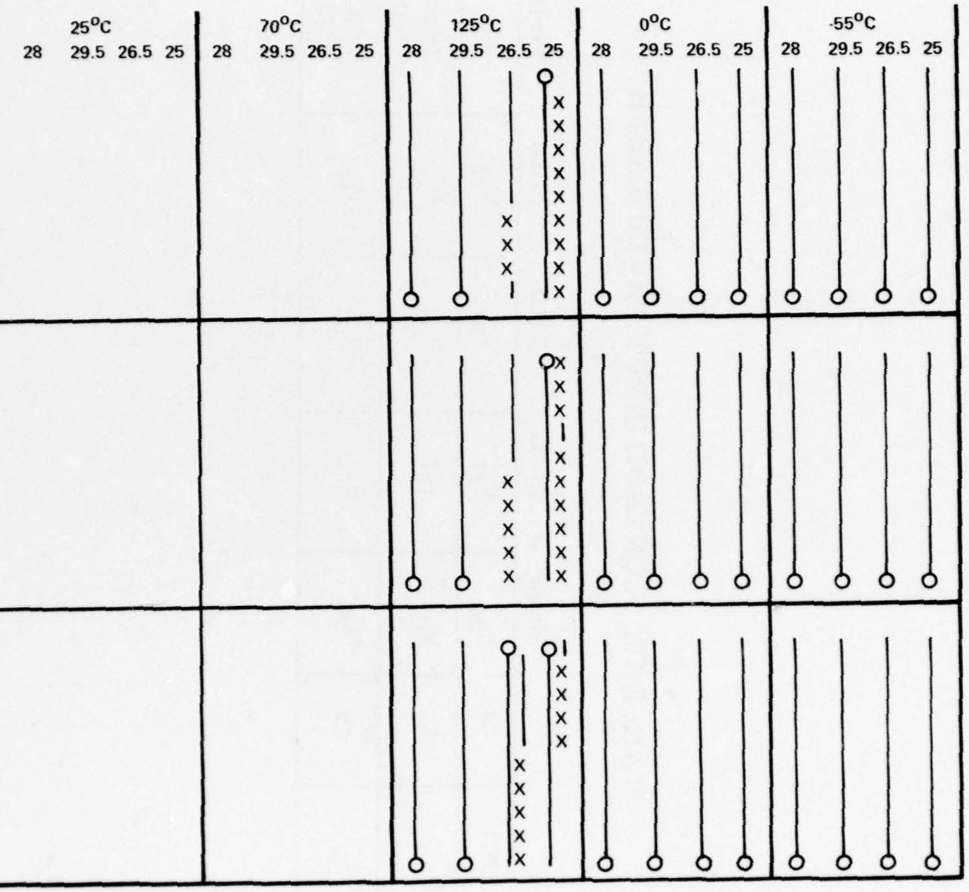
NOTE: DEVICES DELIVERED TO AFAL ARE DESIGNATED BY AF AFTER LOT NO.

TABLE 8.

.5 1 .5 & 1
READ CLOCK PULSE WIDTH

TABLE 9. TEST RESULTS BATCH NO. 4

3			
0	120	5413-4	AF
1	121	5413-4	AF
2	122	5413-4	AF
3	123	5413-4	AF
4	124	5413-4	AF
5	125	5416-2	AF
6	126	5416-2	AF
7	127	5416-2	AF
8	128	5416-2	AF
9	129	5416-2	AF
2			
0	130	5413-4	AF
1	150	5413-4	AF
2	132	5413-4	AF
3	133	5413-4	AF
4	134	5413-4	AF
5	135	5416-2	AF
6	151	5416-2	AF
7	137	5416-2	AF
8	152	5416-2	AF
9	139	5416-2	AF
1			
0	153	5413-4	AF
1	141	5413-4	AF
2	154	5413-4	AF
3	143	5413-4	AF
4	144	5413-4	AF
5	145	5416-2	AF
6	146	5416-2	AF
7	147	5416-2	AF
8	155	5416-2	AF
9	149	5416-2	AF



ALL UNITS OK
6 PM TO 8:30 AM VOLATILITY TEST

READ CLOCK PULSE WIDTH

NOTE: DEVICES DELIVERED TO AFAL ARE DESIGNATED BY AF AFTER LOT NO.

TABLE 10. CONTROL INPUT TRUTH TABLE

		ERASE	WRITE	READ	HOLD	INHIBIT
CHIP SELECT	CS	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{CC}
CONTROL 1	C_1	V_{CC}	V_{CC}	V_{SS}	V_{SS}	DON'T CARE
CONTROL 2	C_2	V_{SS}	V_{CC}	V_{CC}	V_{SS}	DON'T CARE

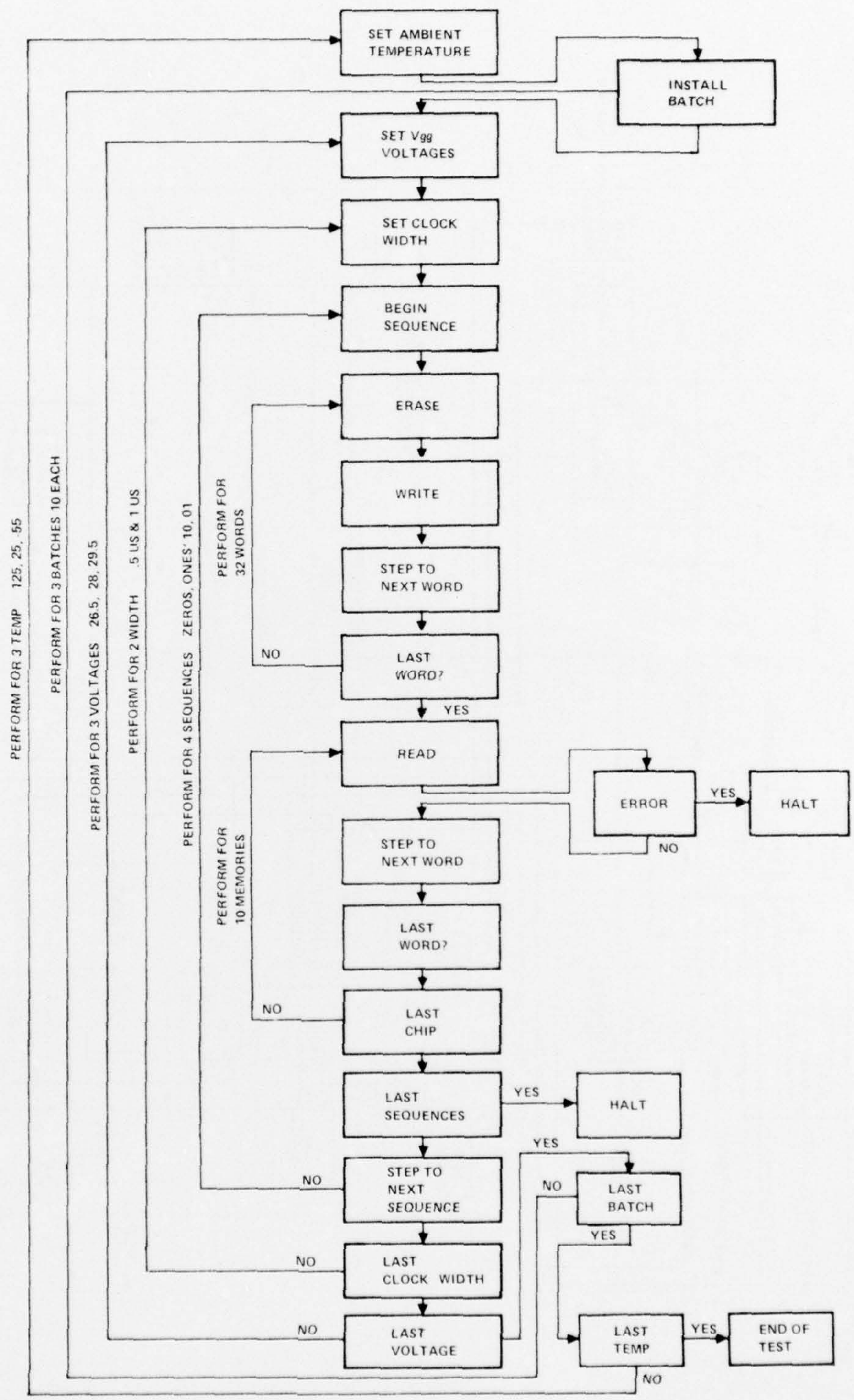


Figure 1. Test Sequence Block Diagram

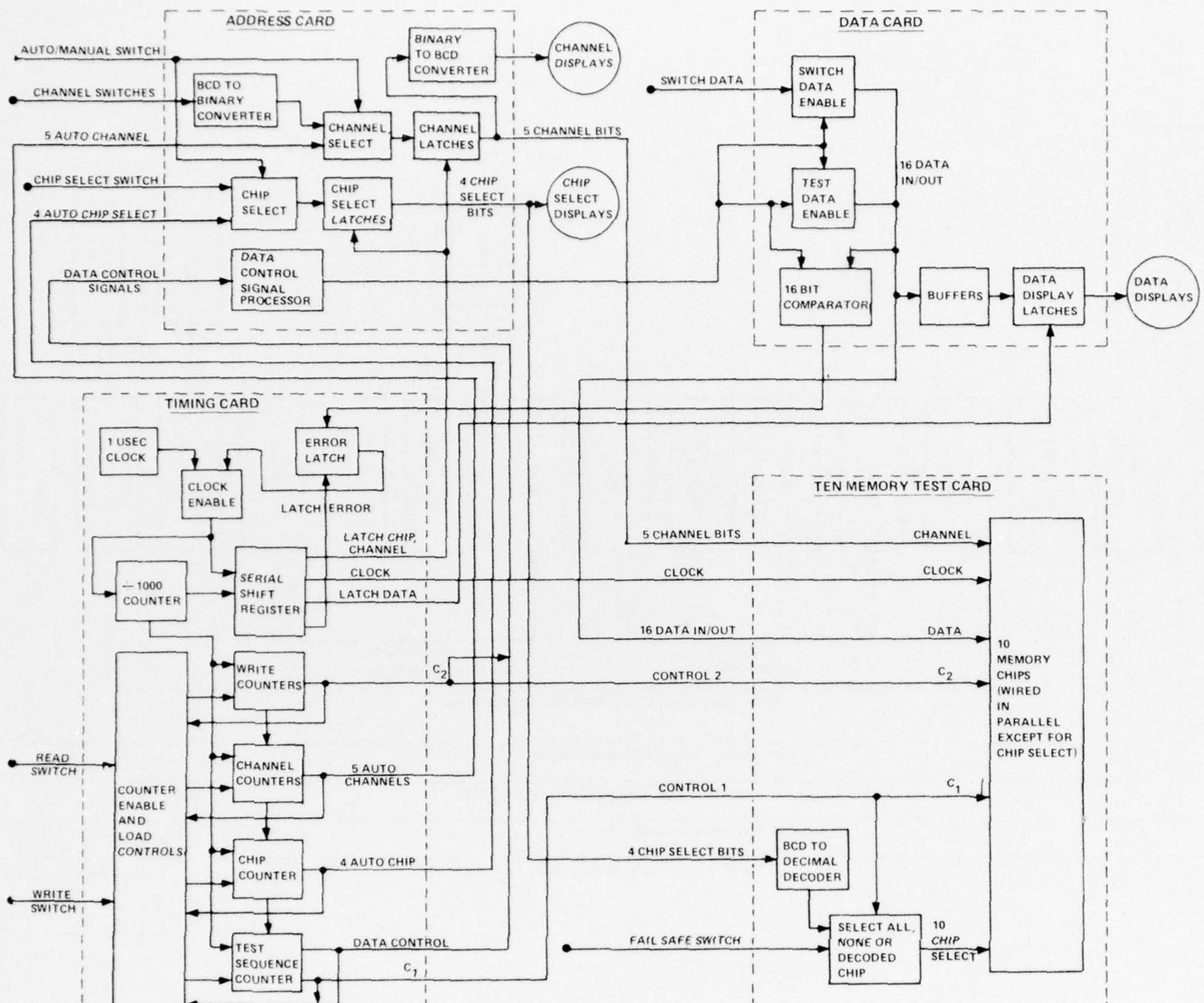


FIGURE B. MEMORY EXERCISER

Figure 2. Memory Exerciser Block Diagram

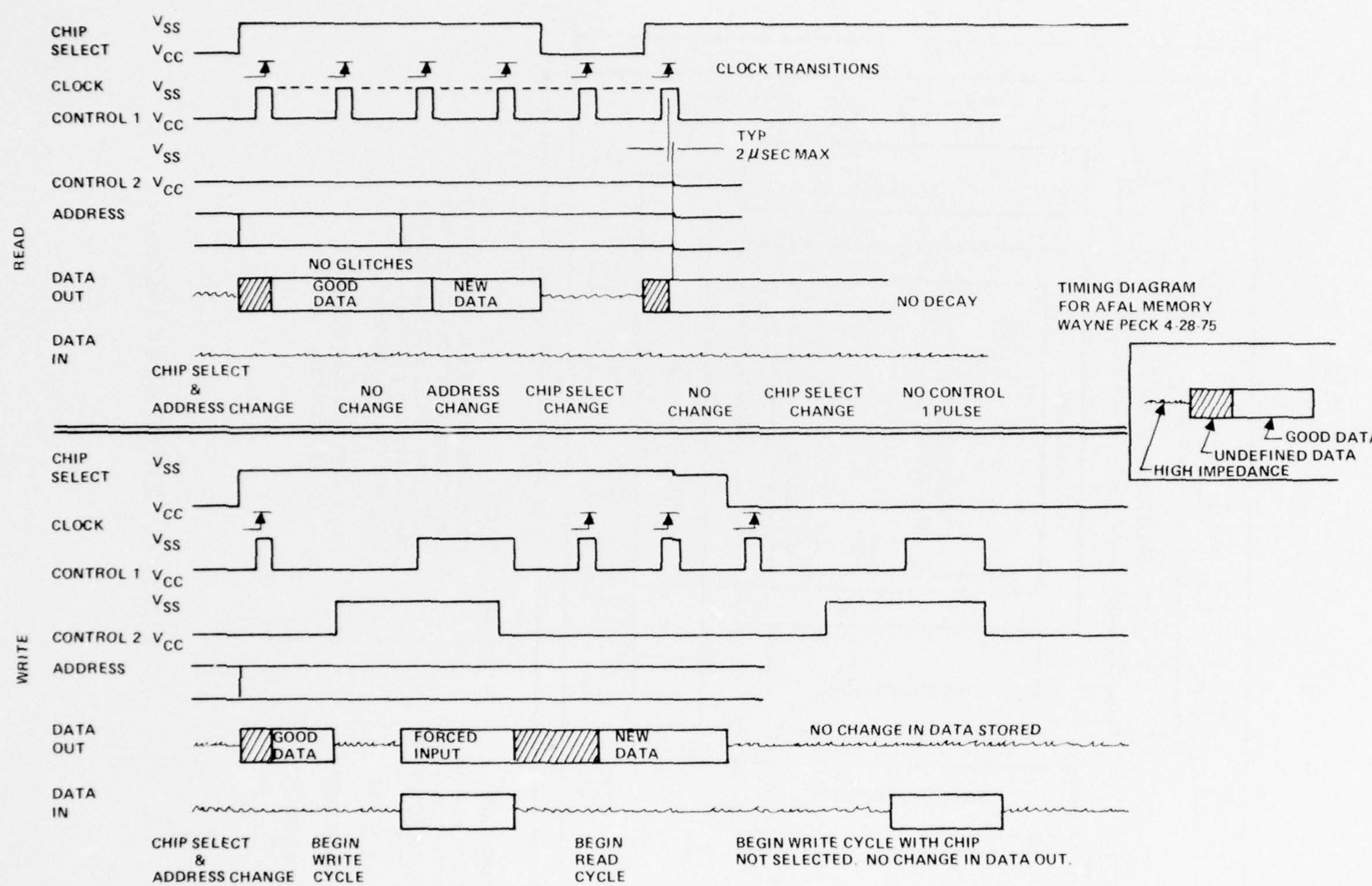
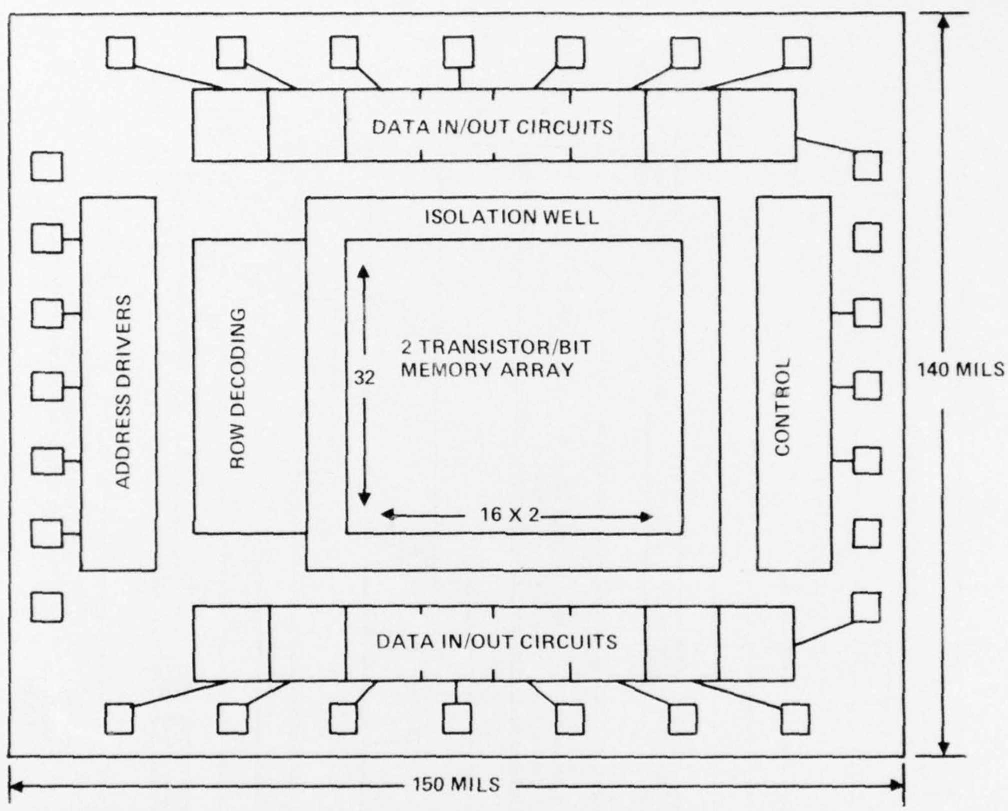


Figure 3. Timing Diagram



FUNCTION	NO. OF PINS	NOTES
DATA IN/OUT	16	CMOS COMPATIBLE 5/10 VOLT SUPPLY
ADDRESS	5	CMOS COMPATIBLE 5/10 VOLT SUPPLY
MODE CONTROL	3	CMOS COMPATIBLE 5/10 VOLT SUPPLY
CLOCK	1	CMOS COMPATIBLE 5/10 VOLT SUPPLY
SUBSTRATE	1	5 ± .5 VOLTS @ 8 MA NOMINAL (10 + .5 VOLTS)
POWER SUPPLY	1	28 ± 1.5 VOLTS @ 8 MA NOMINAL (24 + 1.5 VOLTS)
GROUND	1	
	28	

Figure 4. EROM Block Diagram

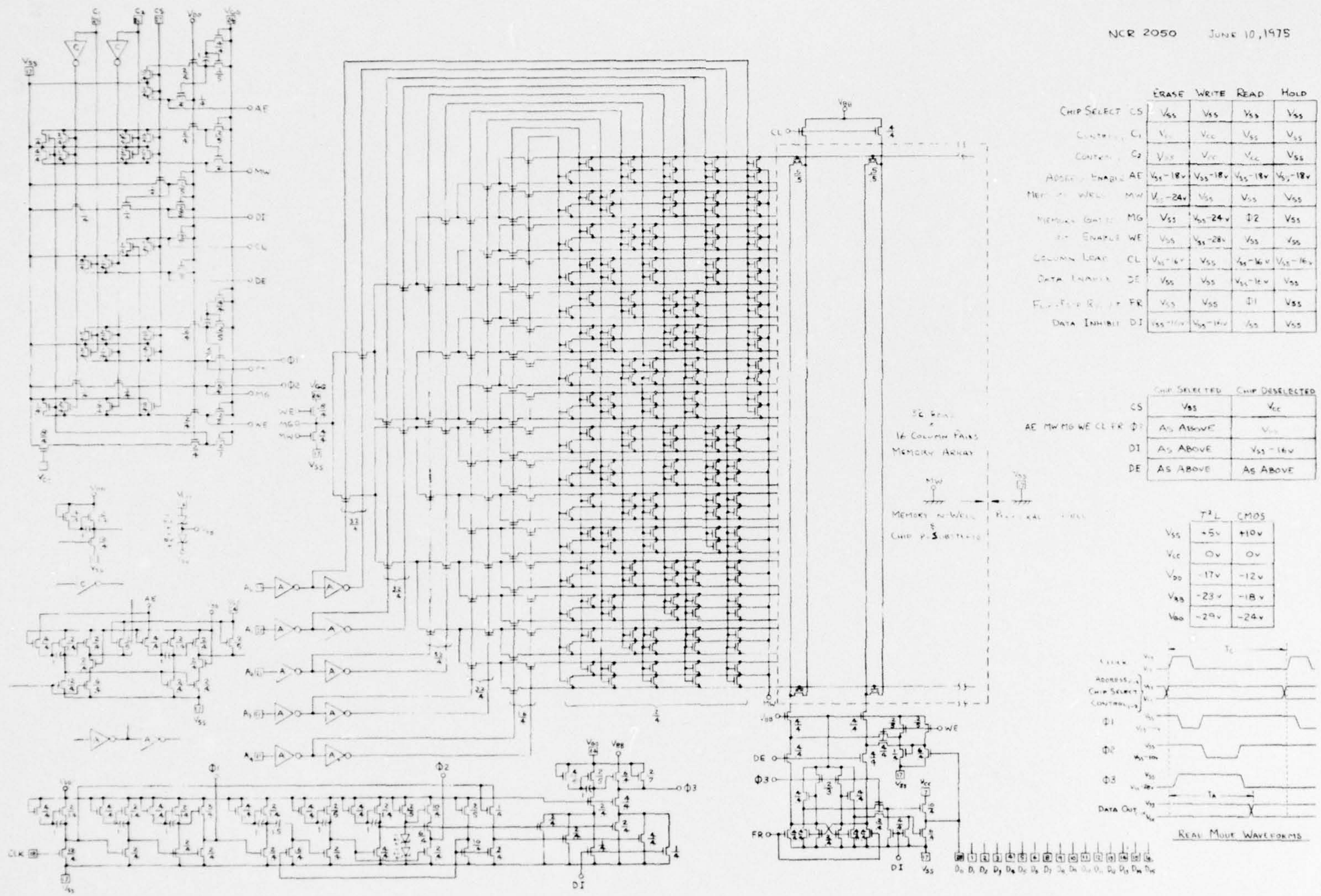


Figure 5. EROM Schematic Diagram

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